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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,487	04/14/2004	Yuuichi Hotta	2102487-991350	8551

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EXAMINER	
DSOUZA, JOSEPH FRANCIS A	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

SF

Office Action Summary	Application No.	Applicant(s)	
	10/825,487	HOTTA, YUUICHI	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 5, 7 - 8, 10 -16, 18 - 19* is/are rejected.

7)☒ Claim(s) *6,9,17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the test clock generator (claim 2) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. The specification states that the test clock is generated externally (page 5, line 11 – 13). No test clock generator is shown in the test circuit.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 5, 10 - 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (US 6,208,621) in view of Igarashi (US 20020140662).

Regarding claim 1, Ducaroir discloses an input/output circuit comprising:

a reference clock generator configured to generate a reference clock (Fig. 1, "reference clock"; Abstract; column 3, line 55 – column 4, line 19);

a signal transmitter configured to transmit serial data in synchronization with one of the reference clock and a test clock (Fig. 1, elements "reference clock", "test clock", mux 16, transmitter 18a; Abstract, 1st 3 lines which indicate serial data transmission; column 4, lines 2 – 4);

a signal-receiving circuit configured to receive the serial data, and to generate a converted signal from the serial data (Fig. 1, receiver 20b; Abstract, 1st 3 lines which

indicate serial data reception; column 1, lines 52 – 65; wherein the converted signal is the recovered clock signal).

Ducaroir does not disclose a test circuit to detect the error between the test clock and the recovered clock.

In the same field of endeavor, however, Igarashi discloses a test circuit configured to detect an error between each phase of the converted signal and the test clock when the signal transmitter operates in synchronization with the test clock (Fig. 1, clock comparator circuit CCM; paragraph 93; wherein the inputs to the CCM are interpreted as the test clock signal and the recovered clock signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Igarashi, in the system of Ducaroir because this would allow the frequency difference between the two clocks to be determined as normal or regular, as disclosed by Igarashi.

Regarding claim 2, Ducaroir discloses the test circuit comprises a test clock generator configured to generate the test clock (Fig. 1, element "test clock"; Abstract; column 4, lines 2 – 4).

Regarding claim 3, Ducaroir discloses the test circuit comprises a selector configured to supply one of the test clock and the reference clock to the signal transmitter (Fig. 1, element 16; column 4, lines 2 – 4).

Regarding claim 4, Ducaroir discloses the signal-receiving circuit comprises:

a receiver configured to buffer the serial data (Fig. 1, element 20b);

and a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock (column 1, lines 52 – 65; wherein the converted signal is the recovered clock signal).

Regarding claim 5, Ducaroir does not disclose a clock comparator to compare the test clock signals and recovered clock signal.

In the same field of endeavor, however, Igarashi discloses the test circuit comprises a clock comparator configured to compare the recovery clock with the test clock (Fig. 1, clock comparator circuit CCM; wherein the inputs are interpreted a sthe test clock signal and the recovered clock signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Igarashi, in the system of Ducaroir because this would allow a test clock to be selected for test purposes, as disclosed by Igarashi.

Claims 10 – 16 are similarly analyzed as claims 1, 2, 1, 2, 3, 4, and 5 respectively.

5. Claims 7, 8, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (US 6,208,621) in view of Igarashi (US 20020140662) and further in view of Bonneau et al. (US 20010016929).

Regarding claim 7, Ducaroir discloses the signal-receiving circuit comprises:

a receiver configured to buffer the serial data (Fig. 1, element 20b);

a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock (column 1, lines 52 – 65; wherein the converted signal is the recovered clock signal);

and a deserializer configured to convert the buffered serial data into parallel data in synchronization with the recovery clock (column 5, lines 21 – 24).

Ducaroir does not disclose supplying the parallel data to the test circuit.

In the same field of endeavor, however, Bonneau discloses supplying the parallel data as the converted signal to the test circuit (Fig. 2, element "parallel data out" fed to element "Bist" 216; paragraph 34; wherein the test circuit is interpreted as the Bist circuit that compares the parallel output data with the test pattern).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bonneau, in the system of Ducaroir because this would allow the parallel data to be compared with the test pattern, as disclosed by Bonneau.

Regarding claim 8, Ducaroir does not disclose comparing the parallel data with the test clock.

In the same field of endeavor, however, Bonneau discloses the test circuit comprises a clock comparator configured to compare the parallel data with the test clock (Fig. 1, element 216; paragraph 34; wherein the test clock is interpreted as the test pattern).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bonneau, in the system of Ducaroir because this would allow the parallel data to be compared with the test pattern, as disclosed by Bonneau.

Claims 18 - 19 are similarly analyzed as claims 7 - 8 respectively.

Allowable Subject Matter

Claims 6, 9, 17, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to clock recovery:

Baydar et al. (US 6,333,940) discloses an Integrated digital loop carrier system with virtual tributary mapper circuit.

Tran et al. (US 20020109553) discloses a voltage controlled oscillator that uses a reference clock and clock recovery.

Enam et al. (US 20020114416) discloses phase alignment of data to clock.

Enam et al. (US 20020124030) discloses Integration and hold phase detection circuitry.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

David C. Payne
DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER